DETAILED ACTION

1. This office action is in response to Applicant's amendment filed on January 29, 2008. Claims 1 and 3 have been amended. Claims 1-3 are pending.

Response to Arguments

2. Applicant's arguments filed January 29, 2008 have been fully considered and are persuasive.

Allowable Subject Matter

3. Claims 1-3 are allowed.

The following is an examiner's statement of reasons for allowance:

Applicant Admitted Prior Art (Admission) teaches a security circuit that monitors addresses or instructions read by the CPU and sends an illegitimate access detection signal to the CPU to cause the CPU to perform an adequate process when there has been an access to a program area or a data area an access to which to execute an instruction or write or read data is not permitted; and a test circuit that has a plurality of test signal input terminals provided on the chip but connected to no external circuit with a selector whose switching is controlled by a test mode signal TM. The test circuit gives instructions to the CPU from the test signal input terminals through a probe of testing apparatus at the time of carrying out a production test and causes the CPU to execute a sequence of arbitrary instructions to test if the CPU can properly execute application program or if the peripheral circuit operates properly. (figure 2, page 1, pp. 9-17)

Matsumoto (US 5,657,330) teaches a CPU outputs a predetermined test signals to the output timers according to the test program stored in the test ROM during the test mode, thereby outputting the output signal from the first output timer from the first output timer to the CPU over the corresponding data bus. (col. 13, lines 51-58). Takagi (US 5,280,618) teaches an interrupt test circuit for a microprocessor system which facilitates interrupt performance tests, in which both peripheral and CPU tests can be easily carried out independently and precisely with the minimum time and procedure. (figure 1, col. 2, line 52-col. 3, line 11)

With respect to claim 1: None of the prior art either taken singularly or in combination teach "a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated; a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; and a test circuit which sends a preset specific instruction to said CPU when, in said test mode, a security test signal has been output from said CPU and a specific memory area of said first and second memories has been accessed, wherein the preset specific instruction is provided from a register within said test circuit."

With respect to claim 3: None of the prior art either taken singularly or in combination teach "a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and

accesses said second memory and runs said functional test program when said test mode is designated; a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; and an exception processing circuit, included in said CPU, for executing a predetermined exception process responsive to a signal indicative of an unauthorized illegitimate access of said first and second memories when said functional test program is executing a security test and said memory management unit has instructed execution of said specific operation."

The prior are either taken singularly or in combination fails to anticipate or suggest the above claimed limitations , therefore, the independent claims 1 and 3 are considered to be in condition for allowance as being novel and non-obvious over prior art.

4. Dependent claim 2 is also allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHEWAYE GELAGAY whose telephone number is (571)272-4219. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on 571-272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. G./
Examiner, Art Unit 2137

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2137